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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,907	12/16/2005	Toshinori Sugihara	LB-1035-616	2364

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EXAMINER	
KIM, JAY C	
ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/560,907	SUGIHARA ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to RCE filed April 30, 2009.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 4, it is not clear with respect to what voltage the recited "threshold voltage" is measured, because a voltage is *always* measured with respect to a certain reference voltage; it is not clear how close to “0 V” would be “about 0 V”, because Applicants only disclosed originally “a threshold voltage V_{th} of on the order of 0 V” regarding Fig. 17 of current Application; it is not clear what “a threshold voltage of the semiconductor device” being “restrained” refers to, because a threshold voltage increases over time as shown in Fig. 18 of current Application; if the “threshold voltage of the semiconductor device is restrained” over time as stated in REMARKS filed April 3, 2009, it is not clear whether Applicants claim that the threshold voltage of the semiconductor device is restrained forever and under any operating conditions, which may not be enabling. Claims 5-34 depend on claim 4, and therefore claims 5-34 are also indefinite.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 6, 7, 11, 15-20, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. (US 2003/0047785) in view of Goodman (US 4,204,217) and further in view of Yan et al. (US 2004/0061114).

Regarding claim 4, Kawasaki et al. disclose a semiconductor device (Fig. 1) comprising an active layer (5) (line 3 of [0037]), to which elements are added (lines 3-4 of [0038]), and which is made of a semiconductor containing ZnO or $Mg_xZn_{1-x}O$ (lines 1-3 of [0038]), and a blocking member (4a, 4b, 6, 7 and 9) (lines 3-5 of [0037], [0039], and line 6 of [0050]) for blocking the active layer (5) from an atmosphere such that the atmosphere substantially does not influence a region, in which a movable charge moves, of the active layer (5).

Kawasaki et al. differ from the claimed invention by not showing that nitrogen and hydrogen are added to the active layer, which is made of a semiconductor containing polycrystalline ZnO or $Mg_xZn_{1-x}O$, amorphous ZnO or $Mg_xZn_{1-x}O$, or either mixture of the polycrystalline ZnO and the amorphous ZnO or mixture of the polycrystalline $Mg_xZn_{1-x}O$ and the amorphous $Mg_xZn_{1-x}O$, wherein the nitrogen and hydrogen are intentionally added to the active layer and a threshold voltage of the semiconductor device is restrained to be about 0 V.

Goodman discloses a semiconductor device (Fig. 1) comprising an active layer (16) made of polycrystalline or amorphous ZnO (col. 2, lines 7-9).

Since both Kawasaki et al. and Goodman teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the active layer disclosed by Kawasaki et al. may comprise polycrystalline or amorphous ZnO, because a polycrystalline or amorphous semiconductor material is commonly used in manufacturing a thin film transistor.

Further regarding claim 4, Kawasaki et al. in view of Goodman differ from the claimed invention by not showing that nitrogen and hydrogen are added to the active layer, wherein the nitrogen and hydrogen are intentionally added to the active layer and a threshold voltage of the semiconductor device is restrained to be about 0 V.

Yan et al. disclose that high quality p-type ZnO films can be achieved using either NO or NO_2 gas as a dopant (lines 1-2 of [0036]).

Since both Kawasaki et al. and Yan et al. teach a ZnO semiconductor film, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to dope the active layer disclosed by Kawasaki et al. in view of Goodman with the dopants disclosed by Yan et al., because a high quality ZnO active layer may be formed by using either NO or NO_2 gas as a dopant, and therefore nitrogen is *inherently* added to the active layer.

Further regarding claim 4, Kawasaki et al. in view of Goodman and further in view of Yan et al. differ from the claimed invention by not showing that hydrogen is

intentionally added to the active layer, wherein a threshold voltage of the semiconductor device is restrained to be about 0 V.

It would have been obvious, if not inherent, to the one of ordinary skill in the art at the time the invention was made that the active layer disclosed by Kawasaki et al. in view of Goodman and further in view of Yan et al. may be unintentionally doped with hydrogen, because hydrogen is a common impurity that can unintentionally dope a semiconductor layer in a vacuum chamber or an air ambient via incorporation of hydrogen molecules, organic molecules or water molecules into the semiconductor layer. In this case, a threshold voltage of the semiconductor device is *inherently* restrained to be about 0 V, because Applicants do not specifically define how close to "0 V" would be "about 0 V", and at what point of device operation over time and under what operating conditions the threshold voltage is restrained to be about 0 V.

Further regarding claim 4, the limitation “said nitrogen and hydrogen are intentionally added to the active layer” is a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art unless Applicants specifically claim a concentration of the nitrogen and hydrogen intentionally added to the active layer. Note that a product by process claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a

product by process claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in product by process claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 6 and 7, Kawasaki et al. further disclose for the semiconductor device as set forth in claim 4 that the blocking member (4a, 4b, 6, 7 and 9) is made up of different blocking layers (4a, 4b, 6, 7 and 9) (claim 6), wherein a blocking layer (4b) is made of SiO_2, Al_2O_3, MgO, Ta_2O_5, TiO_2, ZrO_2, CeO_2, K_2O, Li_2O, Na_2O, Rb_2O, In_2O_3, La_2O_3, Sc_2O_3, Y_2O_3, or a solid solution containing at least two of them (lines 5-9 of [0041]) (claim 7).

Regarding claim 11, Kawasaki et al. further comprise for the semiconductor device as set forth in claim 6 a gate electrode (3) (line 4 of [0037]) for controlling move of a movable electric charge in the active layer (5), a gate insulating layer (4), which serves as a block layer, for insulating the active layer (5) from the gate electrode (3), a source electrode (6) connected to the active layer (5), and a drain electrode (7) connected to the active layer (5), wherein a blocking layer (4b) is made of SiO_2, Al_2O_3, MgO, Ta_2O_5, TiO_2, ZrO_2, CeO_2, K_2O, Li_2O, Na_2O, Rb_2O, In_2O_3, La_2O_3, Sc_2O_3, Y_2O_3, or a solid solution containing at least two of them (lines 5-9 of [0041]).

Regarding claims 15-20, 27 and 28, Kawasaki et al. disclose an electronic device (Figs. 8 and 9) comprising, as a switching element (T in Fig. 9), a thin film transistor (Fig. 1) ([0093] and lines 1-3 of [0096]) (claims 15, 17, 19 and 27), wherein the switching element (T) is connected to a picture element electrode (8 in Fig. 1) (line 8 of

[0037]) such that an image signal is written in or read out from the picture element electrode (8) (claims 16, 18, 20 and 28).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. (US 2003/0047785) in view of Goodman (US 4,204,217) and further in view of Yan et al. (US 2004/0061114) as applied to claim 4 above, and further in view of Vijayakumar et al. (US 4,751,149). The teachings of Kawasaki et al. in view of Goodman and further in view of Yan et al. are discussed above.

Kawasaki et al. further disclose that the active layer (5) made of a semiconductor containing ZnO may be formed in an oxygen atmosphere ([0064]), and Yan et al. further comprise the step of forming the active layer under an atmosphere containing NO or NO_2 gas as a dopant (lines 1-2 of [0036]).

Kawasaki et al. in view of Goodman and further in view of Yan et al. differ from the claimed invention by not comprising the step of forming the active layer under an atmosphere containing hydrogen peroxide.

Vijayakumar et al. disclose a method for manufacturing a ZnO thin film (Title), wherein oxygen and hydrogen peroxide can be used as suitable oxidants (col. 2, lines 38-39).

Since both Kawasaki et al. and Vijayakumar et al. teach a ZnO thin film, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the ZnO active layer disclosed by Kawasaki et al. in view of Goodman and further in view of Yan et al. may be formed under an atmosphere containing hydrogen peroxide, because oxygen and hydrogen peroxide may be used interchangeably in

forming a ZnO thin film. Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

6. Claims 8, 12, 21, 22, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. (US 2003/0047785) in view of Goodman (US 4,204,217) and further in view of Yan et al. (US 2004/0061114), and then further in view of Ogawa (US 2002/0056838). The teachings of Kawasaki et al. in view of Goodman and further in view of Yan et al. are discussed above.

Regarding claim 8, Kawasaki et al. further disclose for the semiconductor device as set forth in claim 7 that a blocking layer (9) ([0050]) constituting the blocking layers (4a, 4b, 6, 7 and 9) is made of silicon nitride, and the blocking layer (9) is so provided as to meet the active layer (5) separately from (i) each of two electrodes (6 and 7) serving as blocking layers and connected to the active layer (5), and (ii) an insulating layer (4), which serves as a blocking layer and meets the active layer (5), for insulating the active layer (5) from a control electrode (3) for controlling move of a movable electric charge in the active layer (5).

Kawasaki et al. in view of Goodman and further in view of Yan et al. differ from the claimed invention by not showing that the blocking layer is made of SiO_2, Al_2O_3, MgO, Ta_2O_5, TiO_2, ZrO_2, CeO_2, K_2O, Li_2O, Na_2O, Rb_2O, In_2O_3, La_2O_3, Sc_2O_3, Y_2O_3, …, or a solid solution containing at least two of them.

Ogawa discloses a semiconductor device (Fig. 9) comprising a blocking layer (13) (line 2 of [0181]) for a ZnO semiconductor layer (23) (lines 5-6 of [0177]), wherein the blocking layer (13) can be made of SiO_2 (lines 8-11 of [0077]).

Since both Kawasaki et al. and Ogawa teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to replace the silicon nitride blocking layer disclosed by Kawasaki et al. in view of Goodman and further in view of Yan et al. with the SiO_2 blocking layer disclosed by Ogawa, because SiO_2 is commonly used as an alternative to silicon nitride in manufacturing a semiconductor device.

Regarding claim 12, Kawasaki et al. further disclose for the semiconductor device as set forth in claim 11 that a blocking layer (9) ([0050]) constituting the blocking layers (4a, 4b, 6, 7 and 9) is made of silicon nitride, and the blocking layer (9) is so provided as to meet the active layer (5) separately from the source electrode (6), the drain electrode (7), and the gate insulating layer (4), each of which serves as a blocking layer.

Kawasaki et al. in view of Goodman and further in view of Yan et al. differ from the claimed invention by not showing that the blocking layer is made of SiO_2, Al_2O_3, MgO, Ta_2O_5, TiO_2, ZrO_2, CeO_2, K_2O, Li_2O, Na_2O, Rb_2O, In_2O_3, La_2O_3, Sc_2O_3, Y_2O_3, …, or a solid solution containing at least two of them.

Ogawa discloses a semiconductor device (Fig. 9) comprising a blocking layer (13) (line 2 of [0181]) for a ZnO semiconductor layer (23) (lines 5-6 of [0177]), wherein the blocking layer (13) can be made of SiO_2 (lines 8-11 of [0077]).

Since both Kawasaki et al. and Ogawa teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to replace the silicon nitride blocking layer disclosed by Kawasaki et al. in view of Goodman and further in view of Yan et al. with the SiO_2 blocking layer disclosed by Ogawa, because SiO_2 is commonly used as an alternative to silicon nitride in manufacturing a semiconductor device.

Regarding claims 21, 22, 29 and 30, Kawasaki et al. disclose an electronic device (Figs. 8 and 9) comprising, as a switching element (T in Fig. 9), a thin film transistor (Fig. 1) ([0093] and lines 1-3 of [0096]) (claims 21 and 29), wherein the switching element (T) is connected to a picture element electrode (8 in Fig. 1) (line 8 of [0037]) such that an image signal is written in or read out from the picture element electrode (8) (claims 22 and 30).

7. Claims 9, 10, 13, 14, 23-26 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. (US 2003/0047785) in view of Goodman (US 4,204,217) and further in view of Yan et al. (US 2004/0061114), and then further in view of Kaneko et al. (US 5,166,816). The teachings of Kawasaki et al. in view of Goodman and further in view of Yan et al. are discussed above.

Regarding claims 9 and 10, Kawasaki et al. further disclose for the semiconductor device as set forth in claim 6 that a blocking layer (9) ([0050]) is made of silicon nitride, and the blocking layer (9) is so provided as to meet the active layer (5) separately from (i) each of two electrodes (6 and 7) serving as blocking layers and connected to the active layer (5), and (ii) an insulating layer (4), which serves as a

blocking layer and meets the active layer (5), for insulating the active layer (5) from a control electrode (3) for controlling move of a movable electric charge in the active layer (5).

Kawasaki et al. in view of Goodman and further in view of Yan et al. differ from the claimed invention by not showing that the blocking layer is made of resin.

Kaneko et al. disclose a semiconductor device (Fig. 6), wherein a blocking layer (61) is made of resin (col. 4, line 57), and the blocking layer (61) is so provided as to meet the active layer (54) (col. 4, lines 21-22) separately from each of two electrodes (56 and 57) (col. 4, lines 15-16) serving as blocking layers and connected to the active layer (54), and an insulating layer (53) (col. 4, line 21), which serves as a blocking layer and meets the active layer (54), for insulating the active layer (54) from a control electrode (52) (col. 4, lines 20-21) for controlling move of a movable electric charge in the active layer (54).

Since both Kawasaki et al. and Kaneko et al. teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to replace the blocking layer disclosed by Kawasaki et al. in view of Goodman and further in view of Yan et al. with the polyimide resin disclosed by Kaneko et al., because a polyimide resin is a well-known material for forming an interlayer insulating film in manufacturing a thin film transistor.

Regarding claims 13 and 14, Kawasaki et al. further comprise for the semiconductor device as set forth in claim 6 a gate electrode (3) (line 4 of [0037]) for controlling move of a movable electric charge in the active layer (5), a gate insulating

layer (4), which serves as a block layer, for insulating the active layer (5) from the gate electrode (3), a source electrode (6) connected to the active layer (5), a drain electrode (7) connected to the active layer (5), wherein a blocking layer (9) is made of silicon nitride ([0050]), and the blocking layer (9) is so provided as to meet the active layer (5) separately from the source electrode (6), the drain electrode (7), and the gate insulating layer (4), each of which serves as a blocking layer.

Kawasaki et al. in view of Goodman and further in view of Yan et al. differ from the claimed invention by not showing that the blocking layer is made of a resin.

Kaneko et al. disclose a semiconductor device (Fig. 6) comprising a gate electrode (52) (col. 4, lines 20-21) for controlling move of a movable electric charge in the active layer (54) (col. 4, lines 21-22), a gate insulating layer (53) (col. 4, line 21), which serves as a block layer, for insulating the active layer (54) from the gate electrode (52), a source electrode (57) (col. 4, lines 15-16) connected to the active layer (54), a drain electrode (56) (col. 4, line 16) connected to the active layer (54), wherein a blocking layer (61) is made of a resin (col. 4, line 57), and the blocking layer (61) is so provided as to meet the active layer (54) separately from the source electrode (57), the drain electrode (56), and the gate insulating layer (53), each of which serves as a blocking layer.

Since both Kawasaki et al. and Kaneko et al. teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to replace the silicon nitride blocking layer disclosed by Kawasaki et al. in view of Goodman and further in view of Yan et al. with the polyimide resin disclosed by

Kaneko et al., because a polyimide resin is a well-known material for forming an interlayer insulating film in manufacturing a thin film transistor.

Regarding claims 23-26 and 31-34, Kawasaki et al. disclose an electronic device (Figs. 8 and 9) comprising, as a switching element (T in Fig. 9), a thin film transistor (Fig. 1) ([0093] and lines 1-3 of [0096]) (claims 23, 25, 31 and 33), wherein the switching element (T) is connected to a picture element electrode (8 in Fig. 1) (line 8 of [0037]) such that an image signal is written in or read out from the picture element electrode (8) (claims 24, 26, 32 and 34).

Response to Arguments

8. Applicants' arguments filed April 3, 2009 have been fully considered but they are not persuasive.

Applicants argue that “the claimed device also requires doping with hydrogen to allow "restraint of a TFT property change (threshold voltage shift ΔV_{th}) occurring over time in response to application of a positive voltage, as shown in Fig. 18". Applicants do not specifically claim that the threshold voltage is restrained to be about 0 V over time. Rather, it can be reasonably interpreted that “a threshold voltage of the semiconductor device is restrained to be about 0 V” at a certain time. Also, it is improper to import claim limitations from the specification. See MPEP 2111.01.

Applicants argue that “therefore, the doping of hydrogen in the claimed device must be intentional to ensure that the threshold voltage shift is restrained”, and that “it would not be possible to guarantee this with unintentional doping with hydrogen”. Applicants do not specifically claim ensuring a restrained threshold voltage shift, see the

above response, and therefore it is not clear whether intentional doping of hydrogen is necessary or not. Further, Applicants do not specifically claim a concentration of hydrogen, which may distinguish the claimed invention from unintentional doping of hydrogen.

Applicants argue that "it is submitted that this restraint of the threshold voltage is not disclosed in any of the cited references". See the above response regarding "restraint". Further, Applicants do not specifically claim a reference voltage for the recited threshold voltage, length of time for "restraint" and how close to "0 V" would be "about 0 V" as stated above in rejection of claim 4.

Applicants argue that "therefore, unintentional doping of the active layer with hydrogen would not produce an active layer with the claimed property of having a threshold voltage of about 0 V". See the above responses.

Applicants' arguments, see REMARKS, filed April 3, 2009, with respect to the rejection of claim 5 under Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Yamada have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571) 270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
July 13, 2009
/Kenneth A Parker/
Supervisory Patent Examiner, Art Unit 2815